CLAIMS

1. An apparatus for processing image data to produce an image for covering an image area of a display, comprising:

a plurality of graphics processors, each graphics processor being operable to render the image data into frame image data and to store the frame image data in a respective local frame buffer;

a control processor operable to provide instructions to the plurality of graphics processors; and

one or more merge units operable to synchronously receive the frame image data from the respective local frame buffers and to synchronously produce combined frame image data based thereon.

2. The apparatus of claim 1, wherein at least one of the one or more merge units is operable to produce a merge synchronization signal used by the graphics processors to release the frame image data from the respective local frame buffers to the one or more merge units.

3. The apparatus of claim 2, further comprising:

at least one synchronization unit operable to receive the merge synchronization signal from the at least one merge unit; and

respective local synchronization units coupled to the graphics processors and operable to receive the merge synchronization signal and to cause the release of the frame

image signal from the local frame buffer to the at least one merge unit.

4. The apparatus of claim 2, wherein the merge synchronization signal is synchronized in accordance with a display protocol defining how respective frames of the combined frame image data are to be displayed.

5. The apparatus of claim 4, wherein the display protocol defines at least one of a frame rate at which successive frames of the combined frame image data are displayed, and a blanking period that dictates when the combined frame image data is to be refreshed.

6. The apparatus of claim 5, wherein the merge synchronization signal includes transitions that are proximate to ends of the blanking periods such that the at least one merge unit initiates producing the combined frame image data for display at the end of at least one of the blanking periods.

7. The apparatus of claim 6, wherein the transitions of the merge synchronization signal are substantially coincident with the ends of the blanking periods.

8. The apparatus of claim 6, wherein the merge synchronization signal includes transitions that lead the ends of the blanking periods.

9. The apparatus of claim 2, wherein:

the plurality of graphics processors are grouped into respective sets of graphics processors;

the one or more merge units include a respective local merge unit coupled to each set of graphics processors, and a core merge unit coupled to each local merge unit;

the respective local merge units are operable to synchronously receive the frame image data from the respective local frame buffers and to synchronously produce local combined frame image data based thereon; and

the core merge unit is operable to synchronously receive the local combined frame image data from the respective local merge units and to synchronously produce the combined frame image data based thereon.

10. The apparatus of claim 9, further comprising:

a respective local synchronization unit coupled to each set of graphics processors and to each local merge unit; and

a core synchronization unit coupled each local synchronization unit and to the core merge unit,

wherein the core merge unit is operable to produce the merge synchronization signal used by the core synchronization unit and at least some of the local synchronization units to permit the respective sets of graphics processors to synchronously release the frame image data from the respective local frame buffers to the respective local merge units, and to permit the respective local merge units to synchronously release the local combined frame image data to the core merge unit.

11. The apparatus of claim 9, wherein the control processor is operable to instruct the graphics processors and

the one or more merge units to operate in one or more modes that affect at least one of (i) timing relationships between when image data are rendered, when frame image data are released from respective local frame buffers, and when frame image data are merged; and (ii) how the frame image data are merged to synchronously produce the combined frame image data.

12. The apparatus of claim 11, wherein the core merge unit and the respective local merge units are operatively coupled to the control processor by way of separate control data lines such that exclusive communication between the control processor, the core merge unit, and the respective local merge units at least concerning the instruction to operate in the one or more modes is obtained.

13. An apparatus for processing image data to produce an image for display on a display screen, comprising:

a plurality of graphics processors, each graphics processor being operable to render the image data into frame image data and to store the frame image data in a respective local frame buffer, and each graphics processor including a synchronization counter operable to produce a local synchronization count indicating when the frame image data should be released from the local frame buffer;

a control processor operable to provide instructions to the plurality of graphics processors; and

at least one merge unit operable to synchronously receive the frame image data from the respective local frame buffers and to synchronously produce combined frame image data based thereon.

14. The apparatus of claim 13, wherein the control processor includes a timing generator operable to produce a synchronization signal that is synchronized in accordance with a display protocol defining how respective frames of the combined frame image data are to be displayed.

15. The apparatus of claim 14, wherein the display protocol defines at least one of a frame rate at which successive frames of the combined frame image data are displayed, and a blanking period that dictates when the combined frame image data is to be refreshed.

16. The apparatus of claim 14, wherein the respective synchronization counters one of increment and decrement their synchronization count based on the synchronization signal from the timing generator.

17. The apparatus of claim 16, wherein the graphics processors are further operable to release their respective frame image data to the at least one merge unit when their respective local synchronization counts reach a threshold.

18. The apparatus of claim 17, wherein the instructions from the control processor include respective reset signals indicative of when the respective synchronization counters should reset their respective synchronization count.

19. The apparatus of claim 13, wherein the control processor is operable to instruct the graphics processors to operate in one or more modes that affect at least one of (i) timing relationships between when image data are rendered, when frame image data are released from respective local frame buffers, and when frame image data are merged; and (ii) how

the frame image data are merged to synchronously produce the combined frame image data.

20. The apparatus of claim 19, wherein at least one of the modes provides that:

one or more of the graphics processors completes rendering the image data into the respective frame buffers prior to the end of each blanking period;

one or more of the graphics processors completes rendering the image data into the respective frame buffers prior to the end of an integral number of blanking periods; and

one or more of the graphics processors includes an integral number of local frame buffers and that the one or more graphics processors completes rendering the image data into the respective integral number of frame buffers prior to the ends of a corresponding integral number of blanking periods.

21. The apparatus of claim 19, wherein the modes include at least one of area division, averaging, layer blending, Z-sorting and layer blending, and flip animation.

22. The apparatus of claim 13, wherein:

the plurality of graphics processors are grouped into respective sets of graphics processors;

the at least one merge unit includes a respective local merge unit coupled to each set of graphics processors, and a core merge unit coupled to each local merge unit;

the respective local merge units are operable to synchronously receive the frame image data from the respective local frame buffers and to synchronously produce local combined frame image data based thereon; and

the core merge unit is operable to synchronously receive the local combined frame image data from the respective local merge units and to synchronously produce the combined frame image data based thereon.

23. An apparatus for processing image data to produce an image for covering an image area of a display, comprising:

one or more sets of graphics processors, each graphics processor being operable to render the image data into frame image data and to store the frame image data in a respective local frame buffer;

a control processor operable to provide instructions to the graphics processors;

a data bus operatively coupled to the control processor and the graphics processors;

one or more merge units including one or more local merge units and a core merge unit, a respective one of the local merge units being coupled to each set of graphics processors and being operable to synchronously receive the frame image data from the respective local frame buffers and to synchronously produce local combined frame image data based thereon, and the core merge unit being coupled to each local merge unit and being operable to synchronously receive the local combined frame image data from the respective local

merge units and to synchronously produce the combined frame image data based thereon;

a control data bus operatively coupled to the core merge unit and the local merge units; and

a bus controller operatively coupled between the data bus and the control data bus and operable to transmit and receive data over the data bus and the control data bus on a priority basis.

24. The apparatus of claim 23, wherein the bus controller is an integral part of the core merge unit.

25. The apparatus of claim 23, wherein the control processor is operable to instruct the graphics processors, the local merge unit, and the core merge unit to operate in one or more modes that affect at least one of (i) timing relationships between when image data are rendered, when frame image data are released from respective local frame buffers, and when frame image data are merged; and (ii) how the frame image data are merged to synchronously produce the combined frame image data.

26. The apparatus of claim 25, wherein the control processor communicates at least the instructions concerning the one or more modes of operation to the respective local merge units and the core merge unit by way of the bus controller and the control data bus.

27. The apparatus of claim 23, wherein the core merge unit is operable to produce a merge synchronization signal used by at least some of the graphics processors to synchronously release the frame image data from the respective

local frame buffers to the respective local merge units, and to permit the respective local merge units to synchronously release the local combined frame image data to the core merge unit.

28. The apparatus of claim 27, wherein the core merge unit transmits the merge synchronization signal to the respective graphics processors by way the control data bus, the bus controller, and the data bus.

29. The apparatus of claim 28, wherein the bus controller seizes the data bus when the core merge unit produces the merge synchronization signal such that the merge synchronization signal can be transmitted to the respective graphics processors by way of the data bus on a priority basis.

30. An apparatus for processing image data to produce an image for covering an image area of a display, comprising:

a plurality of sets of graphics processors, each graphics processor being operable to render the image data into frame image data and to store the frame image data in a respective local frame buffer;

a control processor operable to provide instructions to the plurality of graphics processors;

a packet switch operatively coupled to the control processor and the respective sets of graphics processors;

one or more merge units including one or more local merge units and a core merge unit, a respective one of the local merge units being coupled to each set of graphics

processors and being operable to synchronously receive the frame image data from the respective local frame buffers and to synchronously produce local combined frame image data based thereon, and the core merge unit being coupled to each local merge unit and being operable to synchronously receive the local combined frame image data from the respective local merge units and to synchronously produce the combined frame image data based thereon;

a control data bus operatively coupled to the core merge unit and the local merge units; and

a packet switch controller operatively coupled between the packet switch and the control data bus and operable to transmit and receive data over the packet switch and the control data bus on a priority basis.

31. The apparatus of claim 30, wherein the packet switch controller is coupled to the core merge unit by way of a dedicated data line.

32. The apparatus of claim 30, wherein the packet switch controller is an integral part of the core merge unit.

33. The apparatus of claim 32, wherein the control processor is operable to instruct the graphics processors, the local merge unit, and the core merge unit to operate in one or more modes that affect at least one of (i) timing relationships between when image data are rendered, when frame image data are released from respective local frame buffers, and when frame image data are merged; and (ii) how the frame image data are merged to synchronously produce the combined frame image data.

34. The apparatus of claim 33, wherein the control processor communicates at least the instructions concerning the one or more modes of operation to the respective local merge units and the core merge unit by way of the packet switch, the packet switch controller and the control data bus.

35. The apparatus of claim 32, wherein the core merge unit is operable to produce a merge synchronization signal used by at least some of the graphics processors to synchronously release the frame image data from the respective local frame buffers to the respective local merge units, and to permit the respective local merge units to synchronously release the local combined frame image data to the core merge unit.

36. The apparatus of claim 35, wherein the core merge unit transmits the merge synchronization signal to the respective graphics processors by way of the control data bus, the packet switch controller, and the packet switch.

37. The apparatus of claim 36, wherein the packet switch controller seizes the packet switch when the core merge unit produces the merge synchronization signal such that the merge synchronization signal can be transmitted to the respective graphics processors by way of the packet switch on a priority basis.

38. An apparatus for processing image data to produce an image for covering an image area of a display, the apparatus being formed of a subset of a plurality of processing nodes coupled together on a packet-switched network, the apparatus comprising:

at least one accelerator node including a plurality of sets of graphics processors, each graphics processor being operable to render the image data into frame image data and to store the frame image data in a respective local frame buffer;

one or more merge nodes including one or more merge units, the one or more merge units including one or more local merge units and a core merge unit, a respective one of the local merge units being associated with each set of graphics processors and being operable to synchronously receive the frame image data from the respective local frame buffers and to synchronously produce local combined frame image data based thereon, and the core merge unit being associated with each local merge unit and being operable to synchronously receive the local combined frame image data from the respective local merge units and to synchronously produce the combined frame image data based thereon;

at least one configuration node operable to facilitate selecting the subset of processing nodes;

a control node including a control processor operable to provide instructions to the subset of processing nodes over the packet-switched network, and operable to select the subset of processing nodes to participate in processing the image data to produce the image for display; and

at least one packet switch node operable route data packets between the subset of nodes, the data packets forming at least the image data, frame image data, and combined frame image data.

39. The apparatus of claim 38, wherein the configuration node is operable to issue one or more node

configuration requests to the plurality of processing nodes on the packet-switched network, the one or more node configuration requests prompting the processing nodes to transmit at least some information concerning their data processing capabilities and their destination address to the configuration node.

40. The apparatus of claim 39, wherein the at least some information concerning data processing capabilities includes at least one of a rate at which the image data can be processed into frame image data, a number of frame buffers available, frame image data resolution, an indication of respective modes of operation supported by the graphics processors, a number of parallel paths into which respective frame image data may be input for merging into the combined frame image data, an indication of respective modes of operation supported by the merge units, memory size available for storing data, memory access speed, and memory throughput.

41. The apparatus of claim 39, wherein the configuration node is further operable to transmit the destination addresses of substantially all of the processing nodes that responded to the one or more node configuration requests to each of those processing nodes.

42. The apparatus of claim 39, wherein the configuration node is further operable to transmit the information provided by each processing node in response to the one or more node configuration requests and the destination addresses thereof to the control node.

43. The apparatus of claim 42, wherein the control node is operable to select the subset of processing nodes from

among the processing nodes that responded to the one or more node configuration requests to participate in processing the image data to produce the image for display based their responses to the one or more node configuration requests.

44. The apparatus of claim 43, wherein the control node is further operable to transmit a request to participate in processing the image data to produce the image for display to each of the subset of processing nodes prompting them to accept such participation.

45. The apparatus of claim 44, wherein the control node is further operable to transmit one or more further node configuration requests to one or more of the subset of processing nodes that responded to the request to participate.

46. The apparatus of claim 45, wherein the one or more further node configuration requests includes at least a request for the node to provide information concerning a format in which the node expects to transmit and receive at least one of the image data, the frame image data, the combined frame image data, and processing instructions.

47. The apparatus of claim 46, wherein the control node is further operable to determine which of the processing nodes are to be retained in the subset of processing nodes to participate in processing the image data to produce the image for display based on at least one of the data processing capabilities and format information provided in response to the one or more node configuration requests.

48. The apparatus of claim 38, wherein the packet-switched network is formed on a local area network.

49. The apparatus of claim 38, further comprising at least one video hub node operable to (i) receive at least one of a frame of the combined frame image data and at least one externally provided frame of frame image data, (ii) transmit at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data to at least one of the graphics processors such that one or more of the successive frames of frame image data a next frame of the combined frame image data may be based on the at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data.

50. The apparatus of claim 38, wherein the core merge unit is operable to produce a merge synchronization signal used by the graphics processors to release the frame image data from the respective local frame buffers to the local merge units, wherein the merge synchronization signal is synchronized in accordance with a display protocol defining how respective frames of the combined frame image data are to be displayed.

51. The apparatus of claim 50, wherein the display protocol defines at least one of a frame rate at which successive frames of the combined frame image data are displayed, and a blanking period that dictates when the combined frame image data is to be refreshed.

52. The apparatus of claim 50, wherein the at least one externally provided frame of frame image data adheres to one of the display protocols and the merge synchronization signal is synchronized in accordance with that display protocol such that the core merge unit is operable to produce

a subsequent frame of the combined frame image data based on the at least one externally provided frame of frame image data.

53. The apparatus of claim 38, further comprising at least one memory hub node operable to (i) receive and store common image data, (ii) transmit the common image data to at least one of the graphics processors such that at least one of the successive frames of frame image data and a successive frame of the combined frame image data may include at least some of the common image data.

54. The apparatus of claim 53, wherein the common image data include texture data.

55. The apparatus of claim 38, wherein the packet-switched network is formed on an open network.

56. The apparatus of claim 55, wherein the open network is the Internet.

57. The apparatus of claim 38, wherein the control node is an (n)th level control node, the at least one merge node is an (n)th level merge node, the packet switch node is an (n)th level packet switch node, and at least one accelerator node is an (n)th level accelerator node that includes an (n-1)th level control node and a plurality of (n-1)th level accelerator nodes coupled together by way of an (n-1)th level packet switch node over the packet-switched network.

58. The apparatus of claim 57, wherein at least one of the (n-i)th accelerator nodes includes an (n-i-1)th level control node and a plurality of (n-i-1)th level accelerator

nodes coupled together by way of an (n-i-1)th level packet switch node over the packet-switched network.

59. The apparatus of claim 58, wherein:

at least some of the accelerator nodes are grouped to form respective sets of the graphics processors;

at least some of the merge nodes include respective local merge units associated with the respective sets of the graphics processors such that the respective local merge units are operable to synchronously receive the frame image data from the respective local frame buffers and to synchronously produce local combined frame image data based thereon; and

at least one of the processing nodes of the subset includes a core merge unit operable to synchronously receive the local combined frame image data from the respective local merge units and to synchronously produce the combined frame image data based thereon.

60. The apparatus of claim 59, wherein the (n)th level control node is operable to transmit (n)th level information sets over the packet-switched network to one or more of the subset of processing nodes that at least one of (i) contain instructions, and (ii) contain various data used in the production of the image.

61. The apparatus of claim 60, wherein the instructions include information that causes the graphics processors, the local merge units, and the core merge unit to operate in one or more modes that affect at least one of (i) timing relationships between when image data are rendered, when frame image data are released from respective local frame

buffers, and when frame image data are merged; and (ii) how the frame image data are merged to synchronously produce the combined frame image data.

62. The apparatus of claim 60, wherein the various data used in the production of the image includes at least one of texture data, video data, and an externally provided frame of frame image data.

63. The apparatus of claim 60, wherein each of the (n)th level information sets includes (i) an (n)th level header indicating that the given information set was issued from the (n)th level control node; (ii) a plurality of (n)th level information blocks, each including information for one or more of the (n)th level nodes.

64. The apparatus of claim 63, wherein the (n)th level packet switch node is operable to route the plurality of (n)th level information blocks to the respective (n)th level nodes.

65. The apparatus of claim 63, wherein at least one of the plurality of (n)th level information blocks includes information for the (n)th level accelerator node.

66. The apparatus of claim 65, wherein the (n)th level information block for the (n)th level accelerator node includes a plurality of respective (n-1)th information sub-blocks for the respective (n-1)th nodes.

67. The apparatus of claim 66, wherein the (n-1)th level packet switch node is operable to route the plurality of (n-1)th level information sub-blocks to the respective (n-1)th level nodes.

68. The apparatus of claim 66, wherein at least one of the (n-i)th level information sub-blocks for an (n-i)th level accelerator node includes a plurality of respective information sub-blocks for respective (n-i-1)th nodes.

69. The apparatus of claim 65, wherein the subset of processing nodes includes at least one (n)th level video hub node operable to (i) receive at least one of a frame of the combined frame image data and at least one externally provided frame of frame image data, (ii) transmit at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data to at least one of the graphics processors such that one or more of the successive frames of frame image data a next frame of the combined frame image data may be based on the at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data.

70. The apparatus of claim 69, wherein at least one of the plurality of (n)th level information blocks includes information for the at least one (n)th level video hub node.

71. The apparatus of claim 65, wherein the subset of processing nodes includes at least one (n)th level memory hub node operable to (i) receive and store common image data, (ii) transmit the common image data to at least one of the graphics processors such that at least one of the successive frames of frame image data and a successive frame of the combined frame image data may include at least some of the common image data.

72. The apparatus of claim 71, wherein at least one of the plurality of (n)th level information blocks includes information for the at least one (n)th level memory hub node.

73. The apparatus of any of claims 1, 23, 30, 38, or 57, wherein the respective local frame buffers of the respective graphics processors are operatively coupled to the one or more merge units by way of separate data lines such that exclusive transmission of the frame image data from the respective local frame buffers to the respective one or more merge units is obtained.

74. The apparatus of any of claims 23, 30, 38, or 57, wherein:

the respective local frame buffers of the respective groups of graphics processors are operatively coupled to the respective local merge units by way of separate data lines such that exclusive transmission of the frame image data from the respective local frame buffers to the respective local merge units is obtained; and

the respective local merge units are operatively coupled to the core merge unit by way of separate data lines such that exclusive transmission of the local combined frame image data from the respective local merge units to the core merge unit is obtained.

75. The apparatus of any of claims 1, 23, 30, 38, or 57, wherein the core merge unit is operable to produce a merge synchronization signal used by at least some of the respective sets of graphics processors to synchronously release the frame image data from the respective local frame buffers to the respective local merge units, and to permit the

respective local merge units to synchronously release the local combined frame image data to the core merge unit.

76. The apparatus of claim 75, wherein the merge synchronization signal is synchronized in accordance with a display protocol defining how respective frames of the combined frame image data are to be displayed.

77. The apparatus of claim 76, wherein the display protocol defines at least one of a frame rate at which successive frames of the combined frame image data are displayed, and a blanking period that dictates when the combined frame image data is to be refreshed.

78. The apparatus of claim 77, wherein the merge synchronization signal includes transitions that are proximate to ends of the blanking periods such that the at least one merge unit initiates producing the combined frame image data for display at the end of at least one of the blanking periods.

79. The apparatus of claim 78, wherein the transitions of the merge synchronization signal are substantially coincident with the ends of the blanking periods.

80. The apparatus of claim 78, wherein the merge synchronization signal includes transitions that lead the ends of the blanking periods.

81. The apparatus of claim 75, wherein each of the graphics processors is further operable to render the image data into a respective one of the frame buffers asynchronously with respect to the merge synchronization signal.

82. The apparatus of claim 81, wherein each of the graphics processors is further operable to begin rendering the image data into the respective frame buffers in response to one or more rendering instructions from the control processor.

83. The apparatus of claim 82, wherein at least one of the graphics processors is further operable to issue a rendering complete signal to the control processor when it has completed rendering a frame of the frame image data and to store it in a respective one of the frame buffers.

84. The apparatus of any of claims 1, 23, 30, 38, or 57, wherein the control processor is operable to instruct the graphics processors and the one or more merge units to operate in one or more modes that affect at least one of (i) timing relationships between when image data are rendered, when frame image data are released from respective local frame buffers, and when frame image data are merged; and (ii) how the frame image data are merged to synchronously produce the combined frame image data.

85. The apparatus of claim 84, wherein control processor is operable to instruct the graphics processors and the one or more merge units to operate in the one or more modes on a frame-by-frame basis.

86. The apparatus of claim 84, wherein at least one of the modes provides that:

one or more of the graphics processors completes rendering the image data into the respective frame buffers prior to the end of each blanking period;

one or more of the graphics processors completes rendering the image data into the respective frame buffers prior to the end of an integral number of blanking periods; and

one or more of the graphics processors includes an integral number of local frame buffers and that the one or more graphics processors completes rendering the image data into the respective integral number of frame buffers prior to the ends of a corresponding integral number of blanking periods.

87. The apparatus of claim 84, wherein the modes include at least one of area division, averaging, layer blending, Z-sorting and layer blending, and flip animation.

88. The apparatus of claim 84, wherein at least one of the modes is an area division mode providing that at least two of the local frame buffers are partitioned into respective rendering areas that correspond with respective portions of the image area and non-rendering areas, and an aggregate of the rendering areas results in a total rendering area that corresponds with all portions of the image area.

89. The apparatus of claim 88, wherein the area division mode further provides that the at least two graphics processors complete rendering the image data into the respective rendering areas of the frame buffers prior to the end of each blanking period.

90. The apparatus of claim 88, wherein the one or more merge units are further operable to synchronously aggregate the frame image data from the respective rendering areas of the at least two graphics processors based on alpha

blending values to produce the combined frame image data, and the combined frame image data are capable of covering the image area.

91. The apparatus of claim 84, wherein at least one of the modes is an averaging mode providing that the local frame buffers of at least two of the graphics processors include rendering areas that each correspond with all portions of the image area and that the respective frame image data from the at least two local frame buffers are averaged to produce the combined frame image data.

92. The apparatus of claim 91, wherein the averaging mode further provides that the at least two graphics processors complete rendering the image data into the respective rendering areas of the frame buffers prior to the end of each blanking period.

93. The apparatus of claim 91, wherein the one or more merge unit are further operable to synchronously average the frame image data from the respective rendering areas of the at least two graphics processors based on alpha blending values to produce the combined frame image data, and the combined frame image data are capable of covering the image area.

94. The apparatus of claim 84, wherein at least one of the modes is a layer blending mode providing that: (i) at least some of the image data are rendered into the local frame buffers of at least two of the graphics processors such that each of these local frame buffers includes frame image data representing a portion of the combined frame image data; (ii) each of the portions of the combined frame image data are

prioritized; and (iii) the one or more merge units are further operable to synchronously produce the combined frame image data by layering each of the frame image data in an order according to the priority thereof.

95. The apparatus of claim 94, wherein the one or more merge units are further operable to synchronously layer the frame image data such that one of the layers of frame image data may overwrite another of the layers of frame image data depending on the priority of the layers.

96. The apparatus of claim 94, wherein the layer blending mode further provides that the at least two graphics processors complete rendering the image data into the respective frame buffers prior to the end of each blanking period.

97. The apparatus of claim 84, wherein at least one of the modes is a Z-sorting and layer blending mode providing that: (i) at least some of the image data are rendered into the local frame buffers of at least two of the graphics processors such that each of the at least two local frame buffers includes frame image data representing a portion of the combined frame image data; (ii) the frame image data include Z-values representing image depth; and (iii) the one or more merge units are further operable to synchronously produce the combined frame image data by Z-sorting and layering each of the frame image data in accordance with the image depth.

98. The apparatus of claim 97, wherein the one or more merge units are further operable to synchronously layer the frame image data such that at least a portion of one of

frame image data may overwrite another portion of frame image data depending on the Z-values thereof.

99. The apparatus of claim 97, wherein the Z-sorting and layer blending mode further provides that the at least two graphics processors complete rendering the image data into the respective frame buffers prior to the end of each blanking period.

100. The apparatus of claim 84, wherein at least one of the modes is a flip animation mode providing that: (i) the local frame buffers of at least two graphics processors include frame image data that are capable of covering the image area; and (ii) the one or more merge units are further operable to produce the combined frame image data by sequentially releasing the respective frame image data from the at least two graphics processors.

101. The apparatus of claim 100, wherein the flip animation mode further provides that the at least two graphics processors complete rendering the image data into the respective frame buffers prior to the ends of an integral number of blanking periods.

102. The apparatus of claim 101, wherein the integral number of blanking periods corresponds to the number of graphics processors participating in the flip animation mode.

103. The apparatus of claim 101, wherein the integral number of blanking periods corresponds to the number of local frame buffers participating in the flip animation mode.

104. The apparatus of any of claims 38 or 57, further comprising at least one video hub operable to receive at least one of a frame of the combined frame image data and at least one externally provided frame of frame image data, the at least one video hub being operatively coupled to the plurality of graphics processors such that (i) at least one of the successive frames of frame image data from one or more of the graphics processors may include at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data, and (ii) one or more merge units are operable to produce a successive frame of the combined frame image data based on the at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data.

105. The apparatus of claim 104, wherein the merge synchronization signal is synchronized in accordance with a display protocol defining how respective frames of the combined frame image data are to be displayed.

106. The apparatus of claim 105, wherein the display protocol defines at least one of a frame rate at which successive frames of the combined frame image data are displayed, and a blanking period that dictates when the combined frame image data is to be refreshed.

107. The apparatus of claim 105, wherein the at least one externally provided frame of frame image data adheres to one of the display protocols and the merge synchronization signal is synchronized in accordance with that display protocol such that the merge unit is operable to produce a next frame of the combined frame image data based on

the at least one externally provided frame of frame image data.

108. The apparatus of any of claims 38 or 57, further comprising at least one memory hub operable to receive and store common image data, the at least one memory hub being operatively coupled to the plurality of graphics processors such that (i) at least one of the successive frames of frame image data from one or more of the graphics processors may include at least some of the common image data, and (ii) the one or more merge units are operable to produce a successive frame of the combined frame image data based on the common image data.

109. The apparatus of claim 108, wherein the common image data include texture data.

110. A method for processing image data to produce an image for covering an image area of a display, comprising:

rendering the image data into frame image data using a plurality of graphics processors;

storing the frame image data in respective local frame buffers; and

synchronously merging the frame image data from the respective local frame buffers to synchronously produce combined frame image data based thereon.

111. The method of claim 110, further comprising producing a merge synchronization signal used by at least some of the plurality of graphics processors to synchronously release the frame image data from the respective local frame buffers for merging.

112. The method of claim 111, wherein the merge synchronization signal is synchronized in accordance with a display protocol defining how respective frames of the combined frame image data are to be displayed.

113. The method of claim 112, wherein the display protocol defines at least one of a frame rate at which successive frames of the combined frame image data are displayed, and a blanking period that dictates when the combined frame image data is to be refreshed.

114. The method of claim 113, wherein the merge synchronization signal includes transitions that are proximate to ends of the blanking periods such that the combined frame image data are available for display at the end of at least one of the blanking periods.

115. The method of claim 114, wherein the transitions of the merge synchronization signal are substantially coincident with the ends of the blanking periods.

116. The method of claim 114, wherein the merge synchronization signal includes transitions that lead the ends of the blanking periods.

117. The method of claim 111, wherein the image data are rendered into the respective frame buffers asynchronously with respect to the merge synchronization signal.

118. The method of claim 110, wherein the graphics processors can operate in one or more modes that affect at least one of (i) timing relationships between when image data are rendered, when frame image data are released from

respective local frame buffers, and when frame image data are merged; and (ii) how the frame image data are merged to synchronously produce the combined frame image data.

119. The method of claim 118, further comprising instructing the graphics processors to operate in the one or more modes on a frame-by-frame basis.

120. The method of claim 118, wherein at least one of the modes provides that:

one or more of the graphics processors completes rendering the image data into the respective frame buffers prior to the end of each blanking period;

one or more of the graphics processors completes rendering the image data into the respective frame buffers prior to the end of an integral number of blanking periods; and

one or more of the graphics processors includes an integral number of local frame buffers and that the one or more graphics processors completes rendering the image data into the respective integral number of frame buffers prior to the ends of a corresponding integral number of blanking periods.

121. The method of claim 118, wherein the modes include at least one of area division, averaging, layer blending, Z-sorting and layer blending, and flip animation.

122. The method of claim 118, wherein at least one of the modes is an area division mode providing that at least two of the local frame buffers are partitioned into respective rendering areas that correspond with respective portions of

the image area and non-rendering areas, and an aggregate of the rendering areas results in a total rendering area that corresponds with all portions of the image area.

123. The method of claim 122, wherein the area division mode further provides that the at least two graphics processors complete rendering the image data into the respective rendering areas of the frame buffers prior to the end of each blanking period.

124. The method of claim 122, further comprising synchronously aggregating the frame image data from the respective rendering areas of the at least two graphics processors based on alpha blending values to produce the combined frame image data, and the combined frame image data are capable of covering the image area.

125. The method of claim 118, wherein at least one of the modes is an averaging mode providing that the local frame buffers of at least two of the graphics processors include rendering areas that each correspond with all portions of the image area and that the respective frame image data from the at least two local frame buffers are averaged to produce the combined frame image data.

126. The method of claim 125, wherein the averaging mode further provides that the at least two graphics processors complete rendering the image data into the respective rendering areas of the frame buffers prior to the end of each blanking period.

127. The method of claim 125, further comprising synchronously averaging the frame image data from the respective rendering areas of the at least two graphics

processors based on alpha blending values to produce the combined frame image data, and the combined frame image data are capable of covering the image area.

128. The method of claim 118, wherein at least one of the modes is a layer blending mode providing that: (i) at least some of the image data are rendered into the local frame buffers of at least two of the graphics processors such that each of these local frame buffers includes frame image data representing a portion of the combined frame image data; (ii) each of the portions of the combined frame image data are prioritized; and (iii) the method further comprises synchronously producing the combined frame image data by layering each of the frame image data in an order according to the priority thereof.

129. The method of claim 128, further comprising synchronously layering the frame image data such that one of the layers of frame image data may overwrite another of the layers of frame image data depending on the priority of the layers.

130. The method of claim 128, wherein the layer blending mode further provides that the at least two graphics processors complete rendering the image data into the respective frame buffers prior to the end of each blanking period.

131. The method of claim 118, wherein at least one of the modes is a Z-sorting and layer blending mode providing that: (i) at least some of the image data are rendered into the local frame buffers of at least two of the graphics processors such that each of the at least two local frame

buffers includes frame image data representing a portion of the combined frame image data; (ii) the frame image data include Z-values representing image depth; and (iii) the method further comprises synchronously producing the combined frame image data by Z-sorting and layering each of the frame image data in accordance with the image depth.

132. The method of claim 131, further comprising synchronously layering the frame image data such that at least a portion of one of frame image data may overwrite another portion of frame image data depending on the Z-values thereof.

133. The method of claim 131, wherein the Z-sorting and layer blending mode further provides that the at least two graphics processors complete rendering the image data into the respective frame buffers prior to the end of each blanking period.

134. The method of claim 118, wherein at least one of the modes is a flip animation mode providing that: (i) the local frame buffers of at least two graphics processors include frame image data that are capable of covering the image area; and (ii) the method further comprises producing the combined frame image data by sequentially releasing the respective frame image data from the at least two graphics processors.

135. The method of claim 134, wherein the flip animation mode further provides that the at least two graphics processors complete rendering the image data into the respective frame buffers prior to the ends of an integral number of blanking periods.

136. The method of claim 135, wherein the integral number of blanking periods corresponds to the number of graphics processors participating in the flip animation mode.

137. The method of claim 135, wherein the integral number of blanking periods corresponds to the number of local frame buffers participating in the flip animation mode.

138. The method of claim 110, further comprising:

receiving at least one of a frame of the combined frame image data and at least one externally provided frame of frame image data;

transmitting the at least one of a frame of the combined frame image data and the at least one externally provided frame of frame image data to at least one of the plurality of graphics processors such that (i) at least one of the successive frames of frame image data from one or more of the graphics processors may include at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data; and

producing a successive frame of the combined frame image data based on the at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data.

139. The method of claim 110, further comprising:

receiving and storing common image data in a memory;

transmitting at least some of the common image data to at least some of the plurality of graphics processors such that (i) at least one of the successive frames of frame image

data from one or more of the graphics processors may include at least some of the common image data; and

producing a successive frame of the combined frame image data based on the common image data.

140. The method of claim 139, wherein the common image data include texture data.

141. A method for processing image data to produce an image for display on a display screen, comprising:

rendering the image data into frame image data using a plurality of graphics processors;

storing the frame image data in respective local frame buffers;

producing respective local synchronization counts indicating when the frame image data should be released from the respective local frame buffers; and

synchronously producing combined frame image data from the frame image data.

142. The method of claim 141, further comprising producing a synchronization signal that is synchronized in accordance with a display protocol defining how respective frames of the combined frame image data are to be displayed.

143. The method of claim 142, wherein the display protocol defines at least one of a frame rate at which successive frames of the combined frame image data are displayed, and a blanking period that dictates when the combined frame image data is to be refreshed.

144. The method of claim 142, further comprising one of incrementing and decrementing the respective synchronization counts based on the synchronization signal.

145. The method of claim 144, further comprising releasing the respective frame image data for merging when the respective local synchronization counts reach a threshold.

146. The method of claim 145, further comprising providing respective reset signals indicative of when the respective synchronization counts should be reset.

147. A method for processing image data to produce an image for covering an image area of a display, the method being carried out using a subset of a plurality of processing nodes coupled together on a packet-switched network, the method comprising:

selecting from among the plurality of processing nodes at least one accelerator node including a plurality of sets of graphics processors, each graphics processor being operable to render the image data into frame image data and to store the frame image data in a respective local frame buffer;

selecting from among the plurality of processing nodes one or more merge nodes including one or more merge units, the one or more merge units including one or more local merge units and a core merge unit, a respective one of the local merge units being associated with each set of graphics processors and being operable to synchronously receive the frame image data from the respective local frame buffers and to synchronously produce local combined frame image data based thereon, and the core merge unit being associated with each local merge unit and being operable to synchronously receive

the local combined frame image data from the respective local merge units and to synchronously produce the combined frame image data based thereon;

establishing a control node including a control processor operable to provide instructions to the subset of processing nodes over the packet-switched network, and operable to select the subset of processing nodes to participate in processing the image data to produce the image for display; and

employing at least one packet switch node operable route data packets between the subset of nodes, the data packets forming at least the image data, frame image data, and combined frame image data.

148. The method of claim 147, further comprising issuing one or more node configuration requests to the plurality of processing nodes on the packet-switched network, the one or more node configuration requests prompting the processing nodes to transmit at least some information concerning their data processing capabilities and their destination address to the configuration node.

149. The method of claim 148, wherein the at least some information concerning data processing capabilities includes at least one of a rate at which the image data can be processed into frame image data, a number of frame buffers available, frame image data resolution, an indication of respective modes of operation supported by the graphics processors, a number of parallel paths into which respective frame image data may be input for merging into the combined frame image data, an indication of respective modes of

operation supported by the merge units, memory size available for storing data, memory access speed, and memory throughput.

150. The method of claim 148, further comprising transmitting the destination addresses of substantially all of the processing nodes that responded to the one or more node configuration requests to each of those processing nodes.

151. The method of claim 148, further comprising transmitting the information provided by each processing node in response to the one or more node configuration requests and the destination addresses thereof to the control node.

152. The method of claim 151, further comprising selecting the subset of processing nodes from among the processing nodes that responded to the one or more node configuration requests to participate in processing the image data to produce the image for display based their responses to the one or more node configuration requests.

153. The method of claim 152, further comprising transmitting a request to participate in processing the image data to produce the image for display to each of the subset of processing nodes prompting them to accept such participation.

154. The method of claim 153, further comprising transmitting one or more further node configuration requests to one or more of the subset of processing nodes that responded to the request to participate.

155. The method of claim 154, wherein the one or more further node configuration requests includes at least a request for the node to provide information concerning a format in which the node expects to transmit and receive at

least one of the image data, the frame image data, the combined frame image data, and processing instructions.

156. The method of claim 155, further comprising determining which of the processing nodes are to be retained in the subset of processing nodes to participate in processing the image data to produce the image for display based on at least one of the data processing capabilities and format information provided in response to the one or more node configuration requests.

157. The method of claim 147, wherein the packet-switched network is formed on a local area network.

158. The method of claim 147, further comprising selecting from among the plurality of processing nodes at least one video hub node operable to (i) receive at least one of a frame of the combined frame image data and at least one externally provided frame of frame image data, (ii) transmit at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data to at least one of the graphics processors such that one or more of the successive frames of frame image data a next frame of the combined frame image data may be based on the at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data.

159. The method of claim 155, further comprising selecting from among the plurality of processing nodes at least one memory hub node operable to (i) receive and store common image data, (ii) transmit the common image data to at least one of the graphics processors such that at least one of

the successive frames of frame image data and a successive frame of the combined frame image data may include at least some of the common image data.

160. The method of claim 147, wherein the packet-switched network is formed on an open network.

161. The method of claim 160, wherein the open network is the Internet.

162. The method of claim 147, further comprising establishing a hierarchy among the subset of processing nodes such that the control node is an (n)th level control node, the at least one merge node is an (n)th level merge node, the packet switch node is an (n)th level packet switch node, and at least one accelerator node is an (n)th level accelerator node that includes an (n-1)th level control node and a plurality of (n-1)th level accelerator nodes coupled together by way of an (n-1)th level packet switch node over the packet-switched network.

163. The method of claim 162, wherein at least one of the (n-i)th accelerator nodes includes an (n-i-1)th level control node and a plurality of (n-i-1)th level accelerator nodes coupled together by way of an (n-i-1)th level packet switch node over the packet-switched network.

164. The method of claim 163, further comprising transmitting (n)th level information sets over the packet-switched network to one or more of the subset of processing nodes that at least one of (i) contain instructions, and (ii) contain various data used in the production of the image.

165. The method of claim 164, wherein the instructions include information that causes the graphics processors, the local merge units, and the core merge unit to operate in one or more modes that affect at least one of (i) timing relationships between when image data are rendered, when frame image data are released from respective local frame buffers, and when frame image data are merged; and (ii) how the frame image data are merged to synchronously produce the combined frame image data.

166. The method of claim 164, wherein the various data used in the production of the image includes at least one of texture data, video data, and an externally provided frame of frame image data.

167. The method of claim 164, wherein each of the (n)th level information sets includes (i) an (n)th level header indicating that the given information set was issued from the (n)th level control node; (ii) a plurality of (n)th level information blocks, each including information for one or more of the (n)th level nodes.

168. The method of claim 167, further comprising routing the plurality of (n)th level information blocks to the respective (n)th level nodes.

169. The method of claim 167, wherein at least one of the plurality of (n)th level information blocks includes information for the (n)th level accelerator node.

170. The method of claim 169, wherein the (n)th level information block for the (n)th level accelerator node includes a plurality of respective (n-1)th information sub-blocks for the respective (n-1)th nodes.

171. The method of claim 170, further comprising routing the plurality of (n-1)th level information sub-blocks to the respective (n-1)th level nodes.

172. The method of claim 170, wherein at least one of the (n-i)th level information sub-blocks for an (n-i)th level accelerator node includes a plurality of respective information sub-blocks for respective (n-i-1)th nodes.

173. The method of claim 169, further comprising selecting from among the plurality of processing nodes at least one (n)th level video hub node operable to (i) receive at least one of a frame of the combined frame image data and at least one externally provided frame of frame image data, (ii) transmit at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data to at least one of the graphics processors such that one or more of the successive frames of frame image data a next frame of the combined frame image data may be based on the at least one of the at least one externally provided frame of frame image data and the frame of the combined frame image data.

174. The method of claim 173, wherein at least one of the plurality of (n)th level information blocks includes information for the at least one (n)th level video hub node.

175. The method of claim 169, further comprising selecting from among the plurality of processing nodes at least one (n)th level memory hub node operable to (i) receive and store common image data, (ii) transmit the common image data to at least one of the graphics processors such that at least one of the successive frames of frame image data and a

successive frame of the combined frame image data may include at least some of the common image data.

176. The method of claim 175, wherein at least one of the plurality of (n)th level information blocks includes information for the at least one (n)th level memory hub node.